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26OCT00 E578947-5 D02879
P01/7700 0.00-0026209.7

2. Patent application number *(The Patent Office will fill in this part)* — **0026209.7**

3. Full name, address and postcode of the or of each applicant (*underline all surnames*)

KONINKLIJKE PHILIPS ELECTRONICS N.V.
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5621 BA EINDHOVEN
THE NETHERLANDS

Patents ADP Number (*if you know it*)

If the applicant is a corporate body, give the country/state of its incorporation — THE NETHERLANDS

74929 ~~001~~

4. Title of the invention — DIRECT CONVERSION RADIO TRANSCEIVER

5. Name of your agent (*if you have one*)
"Address for service" in the United Kingdom to which all correspondence should be sent (*including the postcode*)

Andrew G. White
Philips Corporate Intellectual Property
Cross Oak Lane
Redhill
Surrey RH1 5HA

Patents ADP number (*if you know it*) — 71334730002

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Country	Priority Application number (*if you know it*)	Date of filing (*day/month/year*)

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DESCRIPTION

DIRECT CONVERSION RADIO TRANSCEIVER

The invention relates to a radio transceiver, a method of operating a radio transceiver, and an integrated circuit embodying a radio transceiver, each having a low IF receiver and a direct conversion transmitter and suitable for use particularly, but not exclusively, in the 2.4GHz ISM frequency band.

Radio networking standards such as FHSS 802.11 and SWAP-CA require the use of a CSMA (Carrier Sense Multiple Access) protocol in which a radio terminal requiring to transmit must, prior to transmitting, monitor the radio channel on which it wants to transmit to check that it is not being used by another radio terminal. If the channel is in use, the radio terminal will refrain from transmitting. The efficiency of a CSMA protocol is dependent on the speed at which a radio terminal can switch from receive mode to transmit mode. While it is switching it cannot receive and so cannot detect if another radio terminal starts to transmit, which may result in a clash of transmissions. A short receive/transmit switching time is desirable to minimise clashing, thereby maximising radio channel utilisation efficiency.

Radio standards such as FHSS 802.11 require the use of a Time Division Multiple Access protocol in which a radio terminal alternates between transmitting and receiving. Again, a short switching time between receiving and transmitting modes is desirable to minimise the dead time when the radio terminal cannot communicate.

One method of switching between modes is to employ separate local oscillators for the transmitter and the receiver, but this is expensive. A cheaper method of switching between modes is to retune a common oscillator, but this is slow.

The use of highly integrated transceiver architectures is desirable to achieve a low radio terminal cost. One receiver architecture which can be integrated readily is the low IF architecture using a polyphase IF filter. Such an architecture is disclosed in European patent application No. 99944448.2-

2211. Low IF receivers using a polyphase IF filter can be susceptible to interference from a transmitter operating on a nearby frequency. This problem can be accentuated in radio frequency bands such as the 2.4GHz ISM band where there is uncoordinated usage.

One solution for alleviating interference, which is disclosed in European patent application No. 99944448.2-2211, is to switch between high and low side local oscillator (LO) injection frequencies, thereby shifting the image frequency of the receiver. The method disclosed in European patent application No. 99944448.2-2211 for implementing this is to invert the LO signal injected for either the I (In-phase) or the Q (Quadrature) component of the received signal.

It is desirable to reduce the cost of a transceiver by reusing circuits for the transmitter and receiver where possible. One transceiver architecture employing reuse is disclosed in USA patent no. 5,392,460 in which a reference frequency generator common to both transmitter and receiver is employed, although separate frequency synthesisers are used for the transmitter and receiver. In this prior architecture, analogue modulation is applied to the transmitter synthesiser prior to upconversion and digital modulation is applied after upconversion.

Another transceiver architecture also disclosed in USA patent no. 5,392,460 reuses the synthesiser which generates the receiver LO injection signal to also generate the transmitter LO injection signal, but combines this with a second, transmitter synthesiser to mix up to the final transmit carrier frequency. Again, analogue modulation is applied to the transmitter synthesiser prior to upconversion and digital modulation is applied after upconversion.

If either of these architectures disclosed in USA patent no. 5,392,460 were to be used to implement the technique of high/low LO switching disclosed in European patent application No. 99944448.2-2211, or for CSMA, or for TDMA, this would entail switching the receiver synthesiser, which would be slow, resulting in an undesirable period during which reception is not possible.

An object of the invention is to provide an improved transceiver capable of fast switching times and reuse of components between the transmitter and receiver, and suitable for a high level of integration.

According to one aspect of the invention there is a radio transceiver adapted to transmit and receive on a common radio channel in a half duplex mode, comprising a direct conversion transmitter and a low IF receiver, wherein a common frequency generator generates a carrier frequency signal during reception and transmission, a voltage controlled oscillator is modulated by an input signal during transmission, the voltage controlled oscillator generates an offset signal which during reception is at an IF frequency and during transmission is at a modulation deviation frequency, and wherein the offset signal is combined with the carrier frequency signal to generate a local oscillator injection signal during reception and a modulated carrier frequency signal during transmission.

According to a second aspect of the invention there is provided a method of operating a radio transceiver to transmit and receive on a common radio channel in a half duplex mode, comprising transmitting by means of a direct conversion transmitter, receiving by means of a low IF receiver, generating during transmission and reception a carrier frequency signal by means of a common frequency generator, modulating during transmission a voltage controlled oscillator by an input signal, generating an offset signal by means of the voltage controlled oscillator, the offset signal being at an IF frequency during reception and at a modulation deviation frequency during transmission, and combining the offset signal with the carrier frequency signal to generate a local oscillator injection signal during reception and a modulated carrier frequency signal during transmission.

In one embodiment of the invention a signal generator generates an LO signal for both a direct conversion transmitter and a low IF receiver. The signal generator comprises a common frequency generator which generates a signal at a carrier frequency whether the transceiver is in transmit mode or receive mode, and a voltage controlled oscillator (VCO) that operates in different ways depending on whether the transceiver is transmitting or receiving. When the transceiver is in receive mode, the VCO generates a

signal at the low IF which is combined with the carrier frequency signal to generate the LO signal for the receiver. When the transceiver is in transmit mode, the VCO functions as a baseband VCO, being modulated by the input information to be transmitted, and the modulated signal is combined with the carrier frequency signal to generate a modulated carrier for transmission. By this means, switching times between transmit and receive modes are kept short, and reuse of components between transmitter and receiver can be achieved.

In a second embodiment of the invention the receiver LO injection signal may be switched between high side injection and low side injection. By this means interference on the image channel may be alleviated.

In a further embodiment of the invention the VCO is locked to a frequency reference during reception, a control voltage to the locked VCO is sampled, and the sampled control voltage is used to control the modulation deviation frequency during transmission.

In a yet further embodiment of the invention the transceiver is implemented in an integrated circuit.

The invention will now be described, by way of example, with reference to the accompanying drawings wherein;

Figure 1 is a block schematic diagram of one embodiment of a transceiver made in accordance with the invention, and

Figure 2 is a block schematic diagram showing the structure of a signal generator used in the transceiver shown in Figure 1.

Figure 3 contains a table illustrating the transceiver settings required in transmit and receive modes.

Referring to Figure 1, there is a signal generator 2 having an input 3 for input data that is to be transmitted, a first output 4 and a second output 5. The signal delivered to these outputs is dependent on the mode of operation of the transceiver, and is described below. The first output 4 of the signal generator 2 is coupled to a transmitter power amplifier 7, the output of which is coupled to an antenna switch 8. The antenna switch 8 is also connected to

a receiver amplifier 10 and the setting of the antenna switch 8 determines whether an antenna 9 is connected to the output of the transmitter power amplifier 7, when the transceiver is operating in a transmit mode, or to the input of the receiver amplifier 10, when the transceiver is operating in a receive mode. The operation of the antenna switch 8 is controlled by a processor, but for clarity the processor is not illustrated in Figure 1.

The output of the receiver amplifier 10 is coupled to a first input of a first mixer 11 and to a first input of a second mixer 12. A second input of the first mixer 11 is coupled to the first output 4 of the signal generator 2, and a second input of the second mixer 12 is coupled to the second output 5 of the signal generator 2. An output from the first mixer 11, corresponding to the in-phase component of the received signal, is coupled to a first, in-phase signal input of a polyphase IF filter 13. An output from the second mixer 12, corresponding to the quadrature component of the receiver signal, is coupled to a first switchable inverter 16, and an output from the first switchable inverter 16 is coupled to a second, quadrature signal input of the polyphase IF filter 13. First and second, in-phase and quadrature respectively, outputs from the polyphase filter 13 are coupled to in-phase and quadrature signal inputs respectively of a data demodulator 14, which delivers a baseband data signal on an output 15.

Referring to Figure 2, the structure of the signal generator 2 will now be described together with its use to generate various signals required for the transceiver to operate in a transmit mode and in a receive mode.

A frequency reference 25, such as a crystal oscillator, is coupled to a carrier frequency synthesiser 26 which generates an in-phase signal component $\cos\omega_c t$ at the radio carrier frequency ω_c. Alternatively, for fixed frequency applications, a fixed carrier frequency oscillator could be used instead of the frequency reference 25 and carrier frequency synthesiser 26. The in-phase signal component at the carrier frequency is coupled to a 90° phase shifter 28 which delivers on an output a quadrature signal component $\sin\omega_c t$ at the carrier frequency.

There is a voltage controlled oscillator (VCO) 27 which generates an in-phase signal component $\cos\omega_o t$ on a first output 18 and a quadrature signal component $\sin\omega_o t$ on a second output 19 at a variable offset frequency ω_o. Furthermore, by controlling the voltage input to the VCO 27, the VCO 27 may be stopped from oscillating, and reversed such that the quadrature signal component on the second output 19 is inverted to become $-\sin\omega_o t$. Such a VCO is disclosed in International patent application PCT/EP00/00514. The quadrature signal delivered on the second output 19 from the VCO 27 is coupled to a second switchable inverter 36 which can, under processor control, deliver either the non-inverted or inverted version of the quadrature VCO second output 19. For clarity, the processor for controlling the second switchable inverter 36 is not illustrated in Figure 2. Additionally, the quadrature signal output from the second second switchable inverter 36 is coupled to a non-switchable inverter 29.

There is a third mixer 30, a fourth mixer 31, a fifth mixer 32 and a sixth mixer 33 coupled to accept the in-phase and quadrature signal components at the carrier frequency ω_c, delivered by the carrier frequency synthesiser 26 and the 90° phase shifter 28 respectively, and at the VCO frequency ω_o delivered by the second switchable inverter 36 and the non-switchable inverter 29, such that the following products are formed and delivered at the mixer outputs when the VCO 27 is running forwards (thereby delivering $\cos\omega_o t$ and $\sin\omega_o t$ at its first and second outputs 18 and 19 respectively) and second switchable inverter 36 is set to non-invert:

Output of third mixer 30 = $-\sin\omega_c t \times \sin\omega_o t$

Output of fourth mixer 31 = $\cos\omega_c t \times \cos\omega_o t$

Output of fifth mixer 32 = $\sin\omega_c t \times \cos\omega_o t$

Output of sixth mixer 33 = $\cos\omega_c t \times \sin\omega_o t$

The output of the third mixer 30 is coupled to a first input of a first summer 34 and the output of the fourth mixer 31 is coupled to a second input of the first summer 34. The output 4 of the first summer 34 is therefore the in-phase component of the carrier plus VCO frequency i.e.

$$[\cos\omega_c t \times \cos\omega_o t] - [\sin\omega_c t \times \sin\omega_o t] = \cos(\omega_c + \omega_o)t$$

when the VCO 27 is running forwards, thereby delivering $\sin\omega_o t$ at its second output 19, and second switchable inverter 36 is set to non-invert.

The output of the fifth mixer 32 is coupled to a first input of a second summer 35 and the output of the sixth mixer 33 is coupled to a second input of the second summer 35. The output 5 of the second summer 35 is therefore the quadrature component of the carrier plus VCO frequency i.e.

$$[\sin\omega_c t \times \cos\omega_o t] + [\cos\omega_c t \times \sin\omega_o t] = \sin(\omega_c + \omega_o)t$$

when the VCO 27 is running forwards, thereby delivering $\sin\omega_o t$ at its second output 19, and second switchable inverter 36 is set to non-invert.

When the second switchable inverter 36 is set to invert, with the VCO running forwards, the output 4 of the first summer 34 delivers the in-phase component of the carrier minus the VCO frequency i.e.

$$[\cos\omega_c t \times \cos\omega_o t] + [\sin\omega_c t \times \sin\omega_o t] = \cos(\omega_c - \omega_o)t$$

and the output 5 of the second summer 35 delivers the quadrature component of the carrier minus the VCO frequency i.e.

$$[\sin\omega_c t \times \cos\omega_o t] - [\cos\omega_c t \times \sin\omega_o t] = \sin(\omega_c - \omega_o)t$$

The signal components described above are used when the transceiver is in a receive mode, as will be described below. When the transceiver is in a transmit mode the second switchable inverter 36 is set to non-invert and the VCO 27 may be reversed thereby delivering $\cos\omega_o t$ and $-\sin\omega_o t$ at its in-phase and quadrature, first and second outputs 18 and 19 respectively. In this case, the output 4 of the first summer 34 is the in-phase component of the carrier minus VCO frequency i.e.

$$[\cos\omega_c t \times \cos\omega_o t] + [\sin\omega_c t \times \sin\omega_o t] = \cos(\omega_c - \omega_o)t$$

In this way, reversing the VCO 27 has the effect of inverting the frequency deviation on the carrier signal. When the transceiver is in the transmit mode the signal delivered by output 5 of the second summer 35 is not used.

The signals generated at the outputs 4, 5 of the signal generator 2 as required for transmit and receive modes, and the settings of the switchable inverters 16, 36, are summarised in the table of Figure 3.

The frequency reference 25 is coupled to a divider 24 which divides the frequency reference signal down to a low IF frequency. Typically the low IF

frequency is equal to a quarter or half of the channel spacing, but other convenient frequencies may be used. The output of the divider 24 is coupled to a first input of a phase detector 20. The in-phase signal delivered by the first output 18 of the VCO 27 is coupled to a second input of the phase detector 20. An output of the phase detector 20 is coupled to a first input of a selector switch 23, and an output of the selector switch 23 is coupled to a voltage control input of the VCO 27.

Input data supplied to the input 3 of the signal generator 2 is coupled to an input amplifier 22, and an output of the input amplifier 22 is coupled to a second input of the selector switch 23.

Further, the output of the phase detector 20 is coupled to a sample-and-hold circuit 21, and an output of the sample-and-hold circuit 21 is coupled to the input amplifier 22 to control the level of the input signal supplied to the voltage control input of the VCO 27.

When the transceiver is required to operate in receive mode with high side LO injection the following settings are made.

a) The selector switch 23 is set to deliver to its output the signal delivered by the phase detector 20, thereby forming a control loop such that the VCO 27 is locked to the divided frequency reference signal at the low IF frequency.

b) The VCO 27 runs forwards and the second switchable inverter 36 is set to non-invert, such that the generator 2 delivers on outputs 4 and 5 respectively the in-phase and quadrature components of the carrier plus offset frequency which are used as high side LO injection signals by the first and second mixers 11 and 12 respectively.

c) The first switchable inverter 16 is set to non-invert.

If an interfering signal appears on the image channel the receiver is switched to low side LO injection by setting the first and second switchable inverters 16, 36 to invert. By switching the second switchable inverter 36, rather than reversing the VCO 27 to generate $-\sin\omega_o t$, disruption to the frequency locked loop, which could corrupt the received signal, is avoided. Conversely, if interference appears on the image channel when the receiver is set for low side LO injection, the receiver can be switched to high side LO

injection by setting the first and second switchable inverters 16, 36 to non-invert.

When the transceiver is required to operate in transmit mode the following setting are made.

a) The selector switch 23 is set to deliver to its output the input data received from the input amplifier 22, thereby enabling the VCO 27 to be modulated by the input signal and to operate as a baseband VCO. The level of the input signal determines the frequency of the VCO 27 and hence the frequency deviation on the transmitted carrier signal.

b) The sample-and-hold circuit 21 is set to hold (under processor control, not illustrated), thereby enabling the voltage on the sample-and-hold circuit 21 which is sampled during receive mode now to act as a reference to control the input amplifier 22 and hence the deviation frequency provided by the VCO27. In this way, tolerances in the VCO components are compensated for.

c) The second switchable inverter 36 is set to non-invert. The frequency of the signal delivered on the first output 4 of the signal generator 2 is equal to the carrier frequency plus the deviation caused by the input data when the VCO 27 is running forwards, and is equal to the carrier frequency minus the deviation caused by the input data. when the VCO 27 is running backwards.

If desired, the polarity of the deviation may be reversed by setting the second switchable inverter 36 to invert.

In the present specification and claims the word “a” or “an” preceding an element does not exclude the presence of a plurality of such elements. Further, the word “comprising” does not exclude the presence of other elements or steps than those listed.

From reading the present disclosure, other modifications will be apparent to persons skilled in the art. Such modifications may involve other features which are already known in the art of time of arrival estimation and the art of position location systems and which may be used instead of or in addition to features already described herein.

CLAIMS

1. A radio transceiver adapted to transmit and receive on a common radio channel in a half duplex mode, comprising a direct conversion transmitter and a low IF receiver, wherein a common frequency generator generates a carrier frequency signal during reception and transmission, a voltage controlled oscillator is modulated by an input signal during transmission, the voltage controlled oscillator generates an offset signal which during reception is at an IF frequency and during transmission is at a modulation deviation frequency, and wherein the offset signal is combined with the carrier frequency signal to generate a local oscillator injection signal during reception and a modulated carrier frequency signal during transmission.

2. A transceiver as claimed in claim 1, wherein the local oscillator injection signal is switchable between high side and low side injection.

3. A transceiver as claimed in claim 1 wherein the voltage controlled oscillator is locked to a frequency reference during reception, a control voltage to the locked voltage controlled oscillator is sampled, and the sampled control voltage is used to control the modulation deviation frequency during transmission.

4. A method of operating a radio transceiver to transmit and receive on a common radio channel in a half duplex mode, comprising transmitting by means of a direct conversion transmitter, receiving by means of a low IF receiver, generating during transmission and reception a carrier frequency signal by means of a common frequency generator, modulating during transmission a voltage controlled oscillator by an input signal, generating an offset signal by means of the voltage controlled oscillator, the offset signal being at an IF frequency during reception and at a modulation deviation frequency during transmission, and combining the offset signal with the carrier frequency signal to generate a local oscillator injection signal

during reception and a modulated carrier frequency signal during transmission.

5. A method as claimed in claim 4, wherein the local oscillator injection signal is switchable between high side and low side injection.

6. A method as claimed in claim 4, further comprising locking the voltage controlled oscillator to a frequency reference during reception, sampling a control voltage to the locked voltage controlled oscillator, and using the sampled control voltage to control the modulation deviation frequency during transmission.

7. An integrated circuit comprising the radio transceiver as claimed in any one of claims 1 to 3.

8. A radio transceiver constructed and arranged to operate substantially as hereinbefore described with reference to and as shown in the accompanying drawings.

9. A method of operating a radio transceiver substantially as hereinbefore described with reference to the accompanying drawings.

ABSTRACT

DIRECT CONVERSION RADIO TRANSCEIVER

A radio transceiver capable of transmitting and receiving on a common radio channel in a half duplex mode includes a direct conversion transmitter and a low IF receiver. A common frequency generator (26) generates a carrier frequency signal which is used by both the transmitter and receiver and is mixed with the output of a voltage controlled oscillator (27). During reception the voltage controlled oscillator generates a low IF signal which, after mixing with the carrier frequency signal, forms an LO injection signal (4,5). During transmission the VCO is modulated, thereby supplying the modulation on the carrier.

(Figure 2)

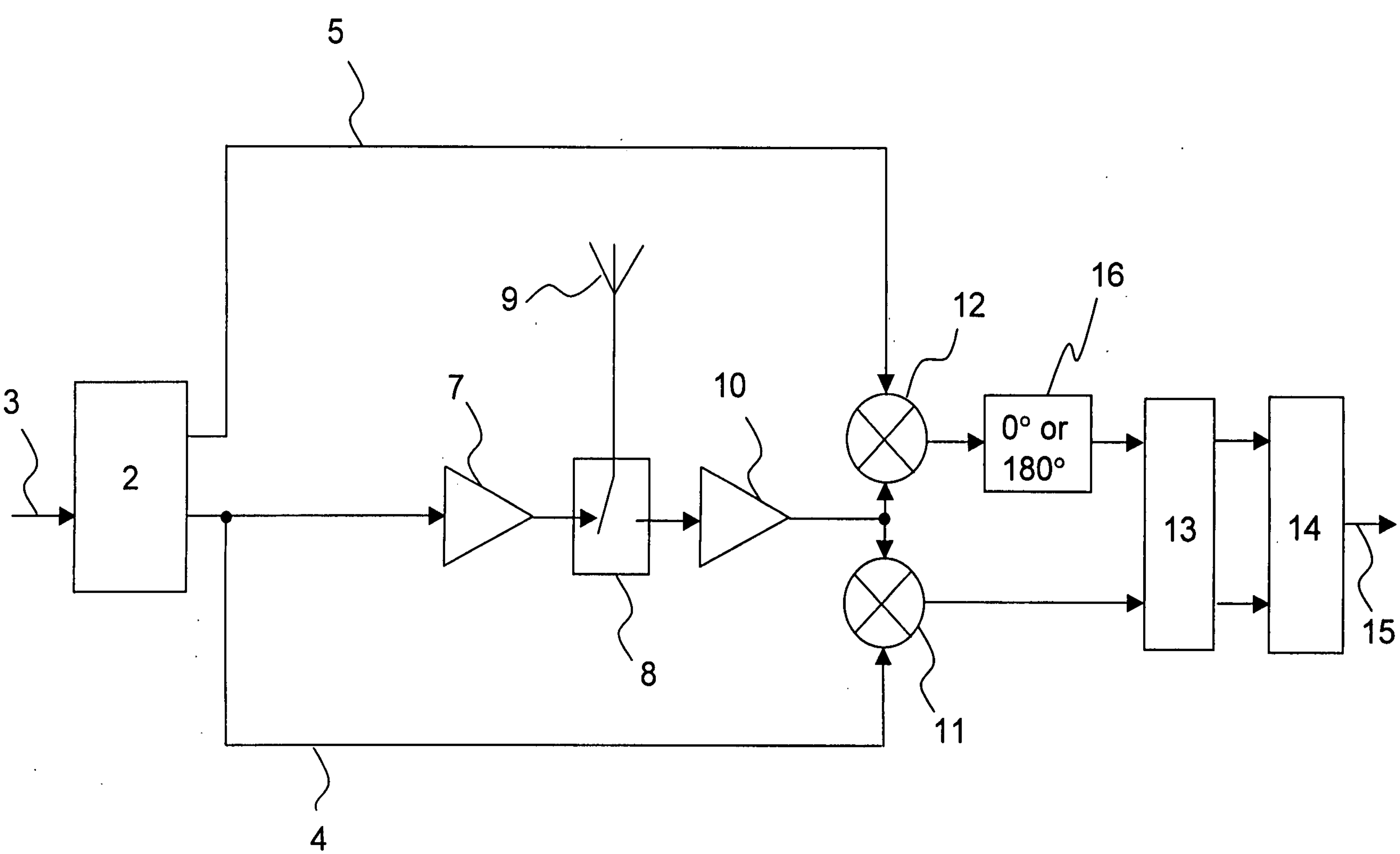

FIG. 1

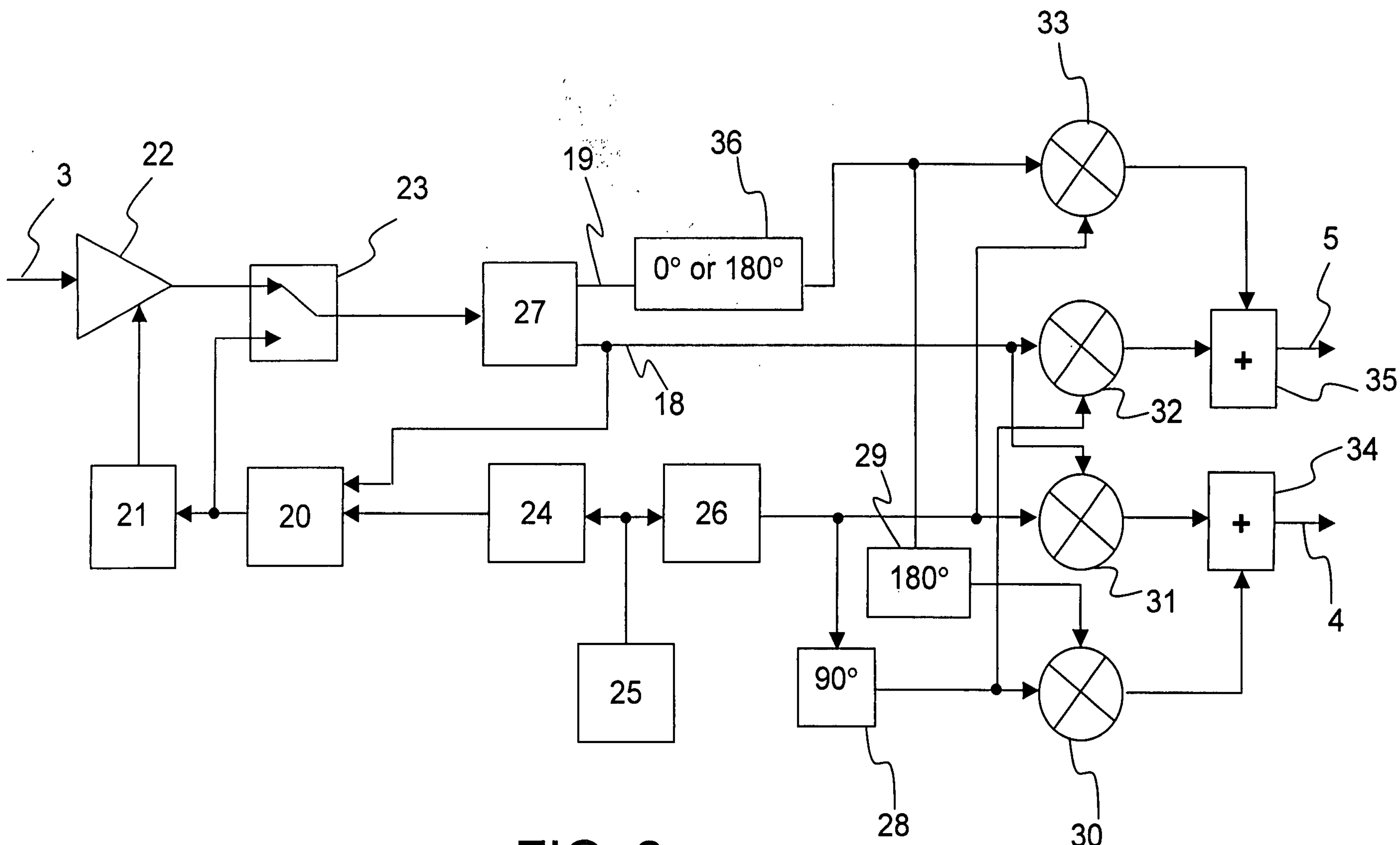
3
22
23
27
19
36
0° or 180°
18
21
20
24
25
26
29
180°
90°
28
33
32
31
30
+
+
5
35
34
4

FIG. 2

Transceiver mode	VCO 27	Second switchable inverter 37	Output 4	Output 5	First switchable inverter 16
Transmit with positive deviation	forward	non-invert	cos $(\omega_c + \omega_o)t$	not used	not used
Transmit with negative deviation	reverse	non-invert	cos $(\omega_c - \omega_o)t$	not used	not used
Receive with high side LO injection	forward	non-invert	cos $(\omega_c + \omega_o)t$	sin $(\omega_c + \omega_o)t$	non-invert
Receive with low side LO injection	forward	invert	cos $(\omega_c - \omega_o)t$	sin $(\omega_c - \omega_o)t$	invert

Fig. 3